IN THE SPECIFICATION

Please replace the existing title with the following new title:

--SEMICONDUCTOR CHIP WHICH COMBINES BULK AND SOI REGIONS AND SEPARATES SAME WITH PLURAL ISOLATION REGIONS--

Page 11, line 19, please amend this paragraph as follows:

(c) Then, as shown in FIG. 3C, a sidewall protection film 25 is formed in order to cover the exposed side face of the SOI layer 23. The sidewall protection film 25 is, for example, silicon nitride (Si_3N_4) or silicon dioxide (SiO_2). After such a material is deposited over the entire surface, only the sidewall protection film 25 is left by RIE. The thickness of the sidewall protection film 25, as well as that of the buried oxide 22 to be removed, are controlled so that the remaining buried oxide 22' is maintained on the base substrate 21 during the formation of the sidewall protection film 25.

Page 17, line 25, please amend this paragraph as follows:

In the second embodiment, the isolation 65c located at the boundary is deeper than the buried oxide 52, and the sidewall protection film 55 and the area containing crystal defect near the boundary are removed altogether when fabricating the isolation. With this arrangement, stress is reduced in the final product, and crystal defect, such as dislocation, is prevented from spreading from the boundary to the epitaxial growth layer 56. Additionally, as shown in FIG. 4, the pn junction of the strap 33 can be positioned deeper than the interface between the base substrate 21 and the epitaxial growth layer 26 for the purpose of reliably separating the pn junction from the interface. Furthermore, the pn junctions of the source and drain of the DRAM cell 43 can be positioned shallower than the interface between the base substrate 21 and the epitaxial growth layer 26. This arrangement can prevent junction leakage and maintain the retention characteristic of the memory cell, even if the interface state deteriorates due to process conditions.

Page 21, line 2 please amend this paragraph as follows:

FIGs. 8A through 8C illustrate an alternative process for fabricating the semiconductor chip 70. In the process shown in FIGs. 7A through 7F, the shallow isolations 75 and 75a were formed only in the SOI device region and at the boundary, and the area that is to be a bulk device region was covered with the mask 74 prior to forming the bulk device region. In the process shown in FIG. 8, isolation 75a is formed over the entire area that is to be the bulk device region.

Page 23, last line, through page 24, line 6, please amend this paragraph as follows:

The first isolation 97a for the DRAM cell 98 is as shallow as the second isolation 97b separating the SOI device 45 in order to reduce the plug resistance of the storage node electrode 29 of the trench capacitor 30. In this manner, isolations in both the bulk device region 11 and the SOI device region 12 are optimized. The fourth isolations 97d for separating the peripheral MOSFETs 94 may be fabricated at the same depth and at the same time as the third isolation 97c using the same material. Alternatively, the fourth isolation 97d may be formed together with the [fist] first and the second isolations 97a and 97b.

Page 27, line 9, please amend this paragraph as follows:

(f) Then, as shown in FIG. 11F, [fist] first isolations 105a positioned in the bulk device region 11, second isolations 105b positioned in the SOI device region12, and a third isolation 105c located at the boundary between the bulk device region 11 and the SOI device region 12 are formed. When forming the third isolation 105c, the sidewall protection film 134 and the surrounding area containing damaged silicon are removed. Although no shown in FIG. 11F, isolations for the peripheral circuit (not shown), which may be formed in the bulk device region 11, are also formed at this stage. The third isolation 105c may be formed by a separate process from the first and second isolations 105a, 105b. Because the width of the second part (i.e., the upper part) of the trench

capacitor 130 formed in the bulk growth layer 106 is relatively small, it is desirable for the first isolation 105a to be as shallow as the second isolation 105b in the SOI device region 12. Alternatively, they may be formed together with the first and second isolations 105a and 105b in the same process for simplicity of the process.

Page 30, line 13, please amend this paragraph as follows:

In the example shown in FIG. 13, the dummy pattern is formed as a dummy capacitor 240 having the same shape and structure as the trench capacitor [240] 230 of the DRAM cell 213 positioned in the bulk device region 11. Accordingly, the dummy capacitor 240 is filled with the same material as the storage electrode 229, and has diffusion layer (or lower electrode) 231 and collar dioxide 217. However, the dummy capacitor 240 does not necessarily have diffusion layer 231 or collar dioxide 217. Alternatively, the dummy capacitor 240 may be furnished with isolation, for example, the first isolation 205a, in order to make the dummy electrically inactive.